



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,416	09/24/2003	Varghese George	1678-60-3	9378

996 7590 02/14/2005

GRAYBEAL, JACKSON, HALEY LLP  
155 - 108TH AVENUE NE  
SUITE 350  
BELLEVUE, WA 98004-5901

EXAMINER
----------

CHO, JAMES HYONCHOL

ART UNIT	PAPER NUMBER
----------	--------------

2819

DATE MAILED: 02/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

CT

<b>Office Action Summary</b>	<b>Application No.</b> 10/671,416	<b>Applicant(s)</b> GEORGE, VARGHESE	
	<b>Examiner</b> James Cho	<b>Art Unit</b> 2819	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 September 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 12-25 is/are allowed.
- 6) ☒ Claim(s) 1-4 and 6-8 is/are rejected.
- 7) ☒ Claim(s) 5 and 9-11 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Claim Objections***

Claim 4 is objected to because of the following informalities:

"a configuration" on line 1 appears to be --the configuration--.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4 and 6-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Hunter et al. (US PAT No. 6,834,318).

Regarding claim 1, Figs. 3-5 of Hunter et al. teaches a method of configuring a bidirectional buffer, the buffer (320 in Fig. 3) including first and second nodes (nodes where INDICATOR A, B are present) and the method comprising: applying a configuration signal on one of the first and second signal nodes (INDICATOR A or B is applied to a node); and configuring the buffer responsive to the applied configuration signal (direction of the buffer is configured in response to INDICATOR A/B).

Regarding claim 2, Figs. 3-5 of Hunter et al. teaches the method of claim 1 where configuring the buffer responsive to the applied configuration signal comprises detecting an edge of the applied configuration signal (Fig. 4 shows the voltage change where the edge of the pulse is inherently changed is detected).

Regarding claim 3, Figs. 3-5 of Hunter et al. teaches the method of claim 1 where configuring the buffer responsive to the applied configuration signal comprises detecting a level of the applied configuration signal (Fig. 4 shows the voltage change where the edge of the pulse is inherently changed is detected).

Regarding claim 4, Figs. 3-5 of Hunter et al. teaches the method of claim 1 where applying the configuration signal on one of the first and second nodes comprises selecting one of the signal nodes to which the configuration signal is to be applied where the selected signal node determines a direction of operation of the buffer (during the event 1 in Fig. 4 the change of INDICATOR A is detected and enables buffers A; col. 4, lines 2-4) and applying the configuration signal on the selected node (INDICATOR A is applied to the node).

Regarding claim 6, Figs. 3-5 of Hunter et al. teaches the method of claim 1, where the configuration signal comprises a series of pulses (INDICATOR A in Fig. 4 is a part of series pulse for each data transfer).

Regarding claim 7, Figs. 3-5 of Hunter et al. teaches the method of claim 1 where configuring the buffer responsive to the applied configuration signal comprises enabling the buffer to operate in a first direction with the first signal node corresponding to an input node (during the event 1, buffer 330 is enabled in response to INDICATOR A at the first node. The corresponding node in buffer 330 is a node in BUS A) is enabled and the second node corresponding to an output node (BUS B becomes the output node corresponding to INDICATOR B).

Regarding claim 8, Figs. 3-5 of Hunter et al. teaches a method of configuring a bidirectional buffer, the buffer including first and second signal nodes and the method comprising: applying a configuration signal (INDICATOR A or INDICATOR B) on one of the first and second signal nodes (nodes coupled to INDICATOR A, B) ; storing a first memory bit (A5 stores a bit in response to CK which is driven by INDICATOR A) responsive to the applied configuration signal and enabling the buffer to operate in a first direction responsive to the stored memory bit (direction control output CNTL A, B is on or off in response to an output of A5 in Fig. 5).

#### ***Allowable Subject Matter***

Claims 5 and 9-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 12-25 are allowable over the prior art of record.

Art Unit: 2819

The following is a statement of reasons for the indication of allowable subject matter: Although Hunter et al. (US PAT No. 56,834,318) teaches a bidirectional bus repeater using direction control block, one of ordinary skill in the art would not have been motivated to modify the teaching of Hunter et al. to further includes, among other things, the specific of applying a reset signal to disable the buffer prior to applying the configuration signal on one of the first and second signal nodes required by claim 5, the specifics of storing a second memory bit having a second logic state responsive to storing the memory bit required by claim 9, and the specifics of a detection and configuration circuit coupled to the enable inputs of the buffer circuits and to the two data nodes operable in a configuration mode to configure the buffer circuit in a direction and in a data mode to provide a buffer function as required by claims 12, 21 and 23.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Maugars (US PAT No. 5,923,187) discloses a multidirectional data transmission device.

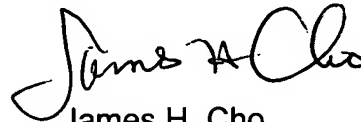
Okazaki (US PAT No. 5,214,330) discloses a bi-directional signal buffering circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

Art Unit: 2819

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



James H. Cho  
Primary Examiner  
Art Unit 2819

Date: 2-8-2005